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TITLE: MONITOR CALIBRATION CIRCUIT

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ABSTRACT:

PROBLEM TO BE SOLVED: To obtain a monitor calibration circuit which calibrates and displays a plurality of monitor points with digital values by one circuit when a plurality of nonlinear voltage and current values are monitored.

SOLUTION: Analog input voltages CH1-CH8 are input to an A/D converter 1 and an output digital monitor signal (b) is stored in a RAM 3 via a data bus. A CPU 2 takes out a digital monitor signal (c) of a designated channel from the RAM 3 and inputs to a calibration process circuit 5. The calibration process circuit 5 executes a calibration process with using a calibration data (d) stored in a calibration data EEPROM 4 as a reference monitor value. A calibration output value (c) output from the calibration process circuit 5 is

sent to an LCD display 6 by the CPU 2 through a time sharing process, so that monitor values are displayed together.

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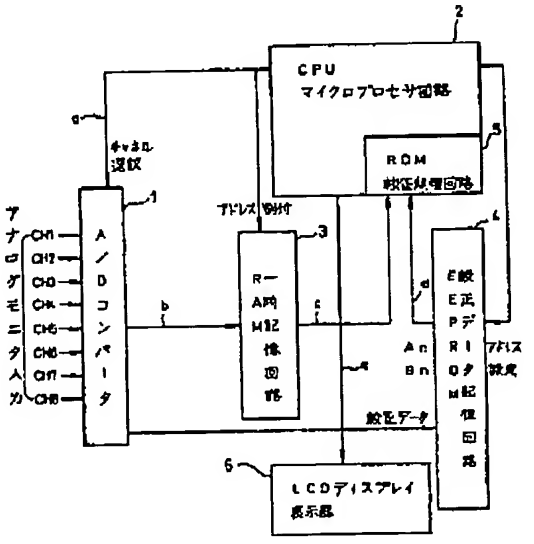
(54)【発明の名称】 モニタ較正回路

(57)【要約】
【課題】 複数の非線形電圧、電流値のモニタに際し、ディジタル値にて一回路でもって複数モニタ点の較正を行い、表示するモニタ較正回路を得る。
【解決手段】 アナログ入力電圧ＣＨ１～ＣＨ８はＡ／Ｄコンバータ１に入力され、出力されたディジタルモニタ信号ｂはデータバスを介してＲＡＭ３に記憶される。ＣＰＵ２は指定チャネルのディジタルモニタ信号ｃをＲＡＭ３より取出し、較正処理回路５に入力する。較正処理回路５は較正データＥＥＰＲＯＭ４に記憶されている較正データｄを使用し、これを基準モニタ値として較正処理を行う。較正処理回路５より出力された較正出力値ｅはＣＰＵ２によりＬＣＤディスプレイ６へ時分割処理にて送られ各モニタ値を一括表示する。



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【特許請求の範囲】

【請求項1】 複数のアナログモニタ入力信号を時分割にてディジタルモニタ信号に変換するA／D変換手段と、前記ディジタルモニタ信号を一時記憶する一時記憶手段と、前記ディジタルモニタ信号を較正する較正データを格納する較正データ格納手段と、前記一時格納手段から読み出された前記ディジタルモニタ信号を対応する前記較正データを基に較正する較正処理手段と、前記複数のアナログモニタ入力信号に対応する複数の較正されたディジタルモニタ信号を時分割にて入力し一括表示する表示手段とを含むことを特徴とするモニタ較正回路。

【請求項2】 前記較正処理手段は、前記ディジタルモニタ信号を線形近似により較正することを特徴とする請求項1記載のモニタ較正回路。

【請求項3】 前記較正データ格納手段は、電気的消去可能プログラマブルリードオンリーメモリー素子により構成されることを特徴とする請求項1あるいは2記載のモニタ較正回路。

【請求項4】 前記較正データは、前記A／D変換回路を介して前記較正データ格納手段に格納されることを特徴とする請求項1，2あるいは3記載のモニタ較正回路。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明はモニタ較正回路に関し、特に非線形電圧のモニタ較正回路に関するものである。

【0002】

【従来の技術】従来、非線形な特性を持つ電圧、電流値等のモニタを行う際は、アナログ入力電圧（電流）値毎に、その変化特性に合わせたアナログの逆特性回路を用意し、線形補正した後、アナログメータ表示や、A／Dコンバーターにてディジタル値に変換し、表示回路にて表示あるいはメモリー保存していた。また、ディジタル値に変換した後に線形補正する場合でも、同様に入力信号毎に逆特性の補正回路を用意し、補正していた。

【0003】

【発明が解決しようとする課題】従来のモニタ較正回路は、複数の非線形電圧、電流値のモニタを行う際に、そのモニタする数だけの逆特性補正回路を必要とする問題がある。すなわち、各モニタ値の例えば検出素子の相違や検出方法の違いにより、検出電圧の特性が相違するからである。

【0004】また、複数のモニタを行う際に、スイッチ等にて手動でもってモニタ項目を選択するため、複数のモニタ点（する信号）を同時に表示できない問題がある。すなわち、アナログメータにて同時表示するにはモニタする信号の種類の数だけのメータが必要であり、ディジタル値にて補正していた場合でも複数の逆特性の補正回路を選択するためである。

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【0005】本発明の目的は複数の非線形電圧、電流値のモニタに際し、ディジタル値にて1回路でもって複数モニタ点の較正を行い表示するモニタ較正回路を提供することである。

【0006】

【課題を解決するための手段】本発明によるモニタ較正回路は、複数のアナログモニタ入力信号を時分割にてディジタルモニタ信号に変換するA／D変換手段と、前記ディジタルモニタ信号を一時記憶する一時記憶手段と、前記ディジタルモニタ信号を較正する較正データを格納する較正データ格納手段と、前記一時格納手段から読み出された前記ディジタルモニタ信号を対応する前記較正データを基に較正する較正処理手段と、前記複数のアナログモニタ入力信号に対応する複数の較正されたディジタルモニタ信号を時分割にて入力し一括表示する表示手段とを含むことを特徴とする。

【0007】また、前記較正処理手段は前記ディジタルモニタ信号を線形近似により較正することを特徴とし、さらに、前記較正データ格納手段は電気的消去可能プログラマブルリードオンリーメモリー素子により構成されることを特徴とし、さらにまた、前記較正データは前記A／D変換回路を介して前記較正データ格納手段に格納されることを特徴とする。

【0008】本発明の作用は次の通りである。複数のアナログ入力信号をマイクロプロセサ回路からの制御により、時分割にてディジタル値に変換し、一時記憶回路に保存する。また、較正を行うための較正データ記憶回路と表示器を有し、較正処理及び表示器への表示処理は時分割処理を行うマイクロプロセサ回路にて同時に行う。

【0009】アナログ入力信号をマイクロプロセサ回路にて時分割に処理を行うことにより、入力信号毎の逆特性較正回路を用意する必要がない。較正処理を行う回路が1回路のため、高速処理が可能である。時系列処理を高速にて行うことにより、複数のモニタ値を常に更新することが可能であり、複数のモニタ値を液晶ディスプレイ等の表示器にての一括表示が可能となる。

【0010】

【発明の実施の形態】以下に、本発明の実施例について図面を参照して説明する。

【0011】図1は本発明によるモニタ較正回路の実施例の構成を示すブロック図である，図1において、本発明によるモニタ較正回路は、例えば8チャネルのアナログモニタ入力信号CH1～CH8を時分割的にアナログ／ディジタル（A／D）変換するA／Dコンバータ1、モニタ較正回路全体を制御するマイクロプロセサ回路（中央処理装置；CPU；コンピュータ）2、A／Dコンバータの出力のディジタルモニタ信号bを一時記憶するRAM（ランダムアクセスメモリー）3を有する。

【0012】また、較正データを格納するEEPROM（電気的消去可能プログラマブルリードオンリーメモリ

ー：較正データ記憶回路）４、ディジタルモニタ信号ｃを較正データ記憶回路４から読み出された較正データｄを基に較正処理する較正処理回路５、較正されたディジタルモニタ信号ｃを表示する、例えば複数行表示可能な液晶ディスプレイ等の表示器６を有して構成される。

【００１３】本発明の実施例の動作を図１により説明する。図１において、例えば８種類のアナログ入力電圧ＣＨ１～ＣＨ８は、Ａ／Ｄコンバータ１に入力される。ＣＰＵ２はＡ／Ｄコンバータ１にチャネル制御信号ａを入力し、Ａ／Ｄコンバータ１により、指定チャネルのアナログ入力電圧ＣＨ１～ＣＨ８を１６進数（ヘキサデシマル）のディジタル値に変換させ、ディジタルモニタ信号ｂとして出力させる。

【００１４】出力されたディジタルモニタ信号ｂはデータバスを介してＲＡＭ３に記憶される。ＣＰＵ２はディジタルモニタ信号ｂが記憶されるアドレスを指定することにより、他のチャネルのディジタルモニタ信号ｂとの記憶位置が重複しないように管理する。ＣＰＵ２はこの処理を時分割高速処理にて行い、すべてのアナログ入力電圧ＣＨ１～ＣＨ８についてＲＡＭ３にヘキサデシマルデータとして記憶していく。

【００１５】全チャネルのＲＡＭ３へのディジタルモニタ信号ｂの記憶が終了すると、校正処理回路５によるディジタルモニタ信号ｃの較正処理を最初に記憶されたチャネルから開始し、ＲＡＭ３の記憶データを順次更新する。ＣＰＵ２は較正処理回路５により、並列処理あるいは時分割処理にて同時に線形補正処理を行う。ＣＰＵ２は指定チャネルのディジタルモニタ信号ｃをＲＡＭ３より取り出し、ＲＯＭ（リードオンリーメモリー）から成る較正処理回路５に入力する。

【００１６】較正処理回路５は較正データＥＥＰＲＯＭ４に記憶されている較正データｄを使用し、これを基準モニタ値として較正処理を行う。ＥＥＰＲＯＭ４には各モニタ信号ＣＨ１～ＣＨ８に対する較正データが記憶されている。その較正データｄは各モニタ点のフルスケールまでの値を任意の区間に分割し較正点を設けその較正点毎に較正ヘキサデシマルデータを設定している。

【００１７】較正データの一例を図３に示す。図３において、ｎは較正点番号（ｎ＝０，１，２・・・・・ｎ）であり、Ａｎは較正点ｎの１０進数表示データであって、Ｂｎは較正点ｎの１０進数データに対応する１６進数較正データである。ただし、ｈの付加されている数字は１６進数（ヘキサデシマル）の数字であることを示す。　図１に戻って、ＲＯＭから成る較正処理回路５では、最初に入力されたディジタルモニタ信号ｃ（ヘキサデシマルデータ）とＢｎとを比較し、そのデータがどの較正点間に位置するかを算出する。その位置Ｐがｎ＜Ｐ＜ｎ＋１の時、較正処理回路５より出力される較正出力値（Ｍ）ｅはＭ≒Ａｎ＋｛（＜Ｃ＞ｄ－＜Ｂｎ＞ｄ）／（＜Ｂｎ＋１＞ｄ－＜Ｂｎ＞ｄ）｝×（Ａｎ＋１－Ａｎ）となる。ただし、ＣはＲＡＭ３に記憶されているディジタルモニタ信号（ヘキサデシマルデータ）ｃであり、＜　＞ｄは１６進数から１０進数への変換である。

【００１８】その結果、較正出力値（Ｍ）ｅは算出された較正点区間において線形近似される。線形近似例を図２に示す。図２において、較正出力（表示）値（電圧）（Ｖｎ）は較正点データＡｎ（Ｂｎ）に対応し（図３参照）、ディジタルモニタ入力信号Ｃに対応する実線上の点（データ）Ｐは、破線上の点Ｍにて線形近似される。このＰとＭとの差（Ｖｍ－Ｖｐ）がメータ誤差であり、要求されるメータ誤差に合わせて較正点及び較正点数を決定する。

【００１９】図１に戻って、ＲＯＭからなる較正処理回路５への各チャネル毎のディジタルモニタ信号（ヘキサデシマルデータ）ｃの入力はＣＰＵ２により時分割にてＲＡＭ３より入力され、各チャネル毎の較正出力値（Ｍ）ｅを較正処理回路５より出力する。較正処理回路５より出力された較正出力値（Ｍ）ｅはＣＰＵ２によりＬＣＤディスプレイ６へ時分割処理にて送られ、各モニタ値を一括表示する。

【００２０】ＥＥＰＲＯＭ４へのＢｎ（較正点ｎの１０進数表示データに対応する１６進数較正データ）の入力もＡ／Ｄコンバータより行い、ＣＰＵにより直接ＥＥＰＲＯＭ４に記憶される。この動作は各チャンネル毎に実施される。

【００２１】

【発明の効果】以上説明したように本発明は、各モニタ点（チャネル）毎に較正回路を必要とせず１回路にて較正できる効果がある（小型化が可能）。すなわち、較正データ記憶回路に各モニタ点に対する較正点データを記憶しておくことにより、一つの較正計算式にて示される較正処理回路が使用できるからである。

【００２２】また、複数のアナログモニタ入力に対して表示器にモニタ値を一括表示できる効果がある。すなわち、マイクロプロセサ回路にて、高速時分割処理あるいは並列処理を行うからである。

【００２３】さらに、どのような特性の非線形入力に対しても線形近似による較正が可能となる効果がある。すなわち、較正データ記憶回路に記憶するデータの較正点及び較正データを自由に設定可能であるからである。

【００２４】さらにまた、高精度のモニタが可能となる効果がある。すなわち、較正点の位置の選択及び較正点数を増やすことにより、近似特性を真値に近づけることができるからである。

【図面の簡単な説明】

【図１】本発明の実施例のブロック図である。

【図２】線形近似例の一例の説明図である。

【図３】較正データの一例の説明図である。

【符号の説明】

１　Ａ／Ｄコンバータ

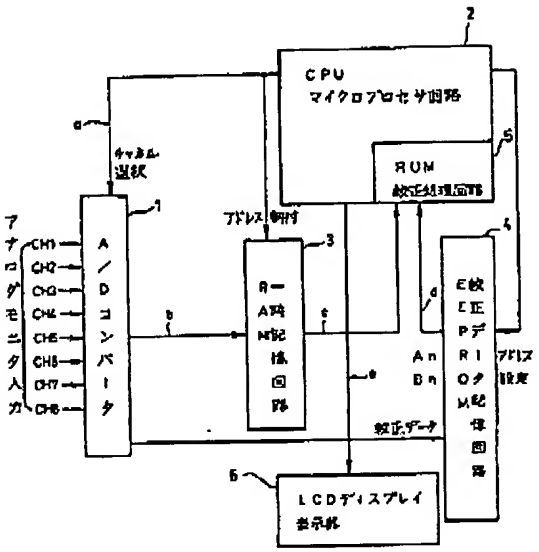
5

2 CPU
3 RAM
4 較正データ記憶回路

6

5 較正処理回路
6 表示器

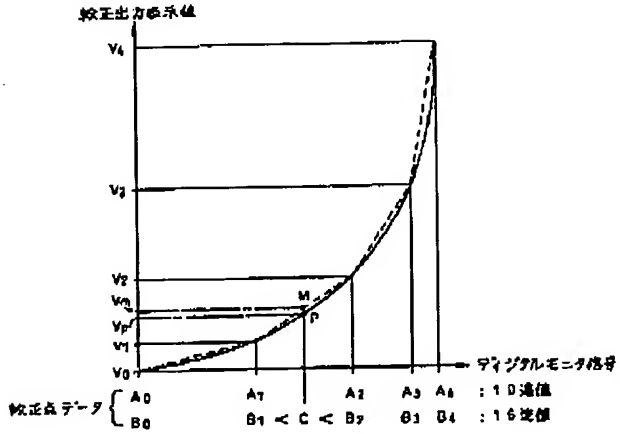
【図1】



【図3】

n	0	1	2	・・・・・・・・	n-1	n
An	0	5	10	・・・・・・・・	95	100
Bn	000h	005h	010h	・・・・・・・・	300h	3FFh
Vn	V0	V1	V2	・・・・・・・・	Vn-1	Vn

【図2】



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CLAIMS

[Claim(s)]
[Claim 1] The monitor calibration circuit characterized by providing the following An A/D-conversion means to change two or more analog monitor input signals into a digital monitor signal in time sharing A memory means to store said digital monitor signal temporarily A calibration data storage means to store the calibration data which proofread said digital monitor signal A calibration processing means to proofread said digital monitor signal by which reading appearance was carried out from said temporary storage means based on said corresponding calibration data, and the display means which inputs the digital monitor signal with which the plurality corresponding to said two or more analog monitor input signals was proofread in time sharing, and indicates by package
[Claim 2] Said calibration processing means is a monitor calibration circuit according to claim 1 characterized by proofreading said digital monitor signal by linear approximation.
[Claim 3] Said calibration data storage means is claim 1 characterized by being constituted by the programmable ROM component eliminable electric, or a monitor calibration circuit given in two.
[Claim 4] Said calibration data are claims 1 and 2 characterized by being stored in said calibration data storage means through said A/D-conversion circuit, or a monitor calibration circuit given in three.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates to the monitor calibration circuit of a nonlinear electrical potential difference about a monitor calibration circuit.
[0002]
[Description of the Prior Art] In case monitors which have a nonlinear property conventionally, such as an electrical potential difference and a current value, were performed, the reverse property circuit of the analog doubled with the change property for every analog input electrical-potential-difference (current) value was prepared, and after carrying out linearity amendment, it changed into digital value with the analog meter display and the A/D converter, and displayed or saved [memory] in the display circuit. Moreover, even when linearity amendment was carried out after changing into digital value, the amendment circuit of a reverse property was similarly prepared and amended for every input signal.
[0003]
[Problem(s) to be Solved by the Invention] In case the conventional monitor calibration circuit performs the monitor of two or more nonlinear electrical potential differences and a current value, it has the problem which needs the number of reverse property amendment circuits which carries out a monitor. That is, it is because the property of a detection electrical potential difference is different with a difference of each monitor value, for example, a sensing element, and the difference in the detection approach.
[0004] Moreover, in case two or more monitors are performed, in order to choose a monitor item as it is also with hand control by a switch etc., there is a problem which cannot display simultaneously two or more monitor points (signal to carry out). That is, a number of the class of signal of meter which carry out a monitor for indicating by simultaneous is required of analog meter, and even when having amended in digital value, it is for choosing the amendment circuit of two or more reverse properties.
[0005] The object of this invention is offering the monitor calibration circuit which proofreads two or more monitor point as it is also in one circuit at digital value, and is displayed on the occasion of the monitor of two or more nonlinear electrical potential differences and a current value.
[0006]
[Means for Solving the Problem] An A/D-conversion means by which the monitor calibration circuit by this invention changes two or more analog monitor input signals into a digital monitor signal in time sharing, A memory means to store said digital monitor signal temporarily, and a calibration data storage means to store the calibration data which proofread said digital monitor signal, A calibration processing means to proofread said digital monitor signal by which reading appearance was carried out from said temporary storage means based on said corresponding calibration data, It is characterized by including the display means which inputs the digital monitor signal with which the plurality corresponding to said two or more analog monitor input signals was proofread in time sharing, and indicates by package.
[0007] Moreover, it is characterized by said calibration processing means proofreading said digital monitor signal by linear approximation, is further characterized by said calibration data storage means

being constituted by the programmable ROM component eliminable electric, and is characterized by storing said calibration data in said calibration data storage means through said A/D-conversion circuit further again.

[0008] The operation of this invention is as follows. By control from a microprocessor circuit, two or more analog input signals are changed into digital value in time sharing, and are saved in a memory circuit. Moreover, it has the calibration data store circuit and drop for proofreading, and calibration processing and display processing to a drop are performed simultaneous in the microprocessor circuit which performs time-sharing processing.

[0009] It is not necessary to prepare the reverse property calibration circuit for every input signal by processing an analog input signal to time sharing in a microprocessor circuit. Since the circuit which performs calibration processing is one circuit, high-speed processing is possible. By performing time series processing at high speed, it is possible to always update two or more monitor values, and the package display of drops, such as a liquid crystal display, is attained in two or more monitor values.

[0010]

[Embodiment of the Invention] Below, the example of this invention is explained with reference to a drawing.

[0011] Drawing 1 is the block diagram showing the configuration of the example of the monitor calibration circuit by this invention. In drawing 1 , the monitor calibration circuit by this invention has A/D converter 1 which carries out the analog / digital (A/D) conversion of the analog monitor input signals CH1-CH8 of eight channels in time sharing, the microprocessor circuit (central processing unit;CPU; computer) 2 which controls the whole monitor calibration circuit, and RAM (random access memory)3 which stores temporarily the digital monitor signal b of the output of an A/D converter.

[0012] Moreover, the calibration processing calibration processing circuit 5 based on EEPROM (a programmable ROM eliminable electric; calibration data store circuit)4 which stores calibration data, and the calibration data d by which reading appearance was carried out from the calibration data store circuit 4 in the digital monitor signal c, and the proofread digital monitor signal e are displayed, for example, it has the drops 6, such as a liquid crystal display in which a multi-line display is possible, and is constituted.

[0013] Drawing 1 explains actuation of the example of this invention. In drawing 1 , eight kinds of analog input electrical potential differences CH1-CH8 are inputted into A/D converter 1. CPU2 inputs the channel-control signal a into A/D converter 1, transforms the analog input electrical potential differences CH1-CH8 of an assignment channel to the digital value of a hexadecimal (hexa decimal), and is made to output as a digital monitor signal b by A/D converter 1.

[0014] The outputted digital monitor signal b is memorized by RAM3 through a data bus. By specifying the address with which the digital monitor signal b is memorized, CPU2 is managed so that the storage location with the digital monitor signal b of other channels may not overlap. CPU2 performs this processing by time-sharing high-speed processing, and memorizes it as hexa decimal data to RAM3 about all the analog input electrical potential differences CH1-CH8.

[0015] After storage of the digital monitor signal b to RAM3 of all channels is completed, calibration processing of the digital monitor signal c by the proofreading processing circuit 5 is started from the channel memorized first, and renewal of sequential of the stored data of RAM3 is carried out. By the calibration processing circuit 5, CPU2 performs linearity amendment processing simultaneously by parallel processing or time-sharing processing. CPU2 inputs the digital monitor signal c of an assignment channel into the calibration processing circuit 5 which consists of ejection and ROM (read-only memory) from RAM3.

[0016] The calibration processing circuit 5 uses the calibration data d memorized by the calibration data EEPROM 4, and performs calibration processing by making this into a criteria monitor value. The calibration data to each monitor signals CH1-CH8 are memorized by EEPROM4. The calibration data d divided the value to the full scale of each monitor point at the section of arbitration, established the proofreading point, and has set up calibration hexa decimal data for every proofreading point of the.

[0017] An example of calibration data is shown in drawing 3 . In drawing 3 , n is a proofreading point

number (1 n= 0, 2 ..... n), An is decimal numeral data of the proofreading point n, and Bn is hexadecimal calibration data corresponding to the decimal number data of the proofreading point n. However, it is shown that the figure to which h is added is a figure of a hexadecimal (hexa decimal). It returns to drawing 1 , the digital monitor signals c (hexa decimal data) and Bn inputted first are compared in the calibration processing circuit 5 which consists of ROM, and it computes between which proofreading points the data is located. When the location P is n<P<n +1, the calibration output value (M) e outputted from the calibration processing circuit 5 becomes M=An+{(<C>d-<Bn>d) /(<Bn+1> d-<Bn>d)} x (An+1-An). however, the digital monitor signal (hexa decimal data) c with which C is memorized by RAM3 -- it is -- < -- >d is conversion to a decimal number from a hexadecimal.

[0018] Consequently, in the computed proofreading point section, linear approximation of the calibration output value (M) e is carried out. The example of linear approximation is shown in drawing 2 . In drawing 2 , a calibration output (display) value (electrical potential difference) (Vn) corresponds to the proofreading point data An (Bn) (refer to drawing 3), and linear approximation of the point P on the continuous line corresponding to the digital monitor input signal C (data) is carried out the point M on a broken line. A proofreading point and calibration mark are determined according to the meter error as which the difference (Vm-****) of this P and M is a meter error, and is required.

[0019] Returning to drawing 1 , the input of the digital monitor signal (hexa decimal data) c for every channel to the calibration processing circuit 5 which consists of a ROM is inputted by CPU2 from RAM3 in time sharing, and outputs the calibration output value (M) e for every channel from the calibration processing circuit 5. The calibration output value (M) e outputted from the calibration processing circuit 5 is sent to the LCD display 6 by time-sharing processing by CPU2, and indicates each monitor value by package.

[0020] The input of Bn (hexadecimal calibration data corresponding to the decimal numeral data of the proofreading point n) to EEPROM4 is also performed from an A/D converter, and is memorized by direct EEPROM4 by CPU. This actuation is carried out for every channel.

[0021]

[Effect of the Invention] As explained above, this invention has the effectiveness which does not need a calibration circuit for each monitor point (channel) of every, but can be proofread in one circuit (a miniaturization is possible). That is, it is because the calibration processing circuit shown in one calibration formula can be used by memorizing the proofreading point data to each monitor point to the calibration data store circuit.

[0022] Moreover, the effectiveness which indicates the monitor value by package is shown in a drop to two or more analog monitor inputs. That is, it is because high-speed time-sharing processing or parallel processing is performed in a microprocessor circuit.

[0023] Furthermore, there is effectiveness whose calibration by linear approximation is attained to the nonlinear input of any properties. That is, it is because the proofreading point of data and calibration data which are memorized to a calibration data store circuit can be set up freely.

[0024] There is effectiveness whose monitor of high degree of accuracy becomes possible further again. That is, it is because an approximation property can be brought close to a true value by increasing selection and calibration mark of the location of a proofreading point.

[Translation done.]

* NOTICES *

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TECHNICAL FIELD

[Field of the Invention] Especially this invention relates to the monitor calibration circuit of a nonlinear electrical potential difference about a monitor calibration circuit.

[Translation done.]

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PRIOR ART

[Description of the Prior Art] In case monitors which have a nonlinear property conventionally, such as an electrical potential difference and a current value, were performed, the reverse property circuit of the analog doubled with the change property for every analog input electrical-potential-difference (current) value was prepared, and after carrying out linearity amendment, it changed into digital value with the analog meter display and the A/D converter, and displayed or saved [memory] in the display circuit. Moreover, even when linearity amendment was carried out after changing into digital value, the amendment circuit of a reverse property was similarly prepared and amended for every input signal.

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EFFECT OF THE INVENTION

[Effect of the Invention] As explained above, this invention has the effectiveness which does not need a calibration circuit for each monitor point (channel) of every, but can be proofread in one circuit (a miniaturization is possible). That is, it is because the calibration processing circuit shown in one calibration formula can be used by memorizing the proofreading point data to each monitor point to the calibration data store circuit.
[0022] Moreover, the effectiveness which indicates the monitor value by package is shown in a drop to two or more analog monitor inputs. That is, it is because high-speed time-sharing processing or parallel processing is performed in a microprocessor circuit.
[0023] Furthermore, there is effectiveness whose calibration by linear approximation is attained to the nonlinear input of any properties. That is, it is because the proofreading point of data and calibration data which are memorized to a calibration data store circuit can be set up freely.
[0024] There is effectiveness whose monitor of high degree of accuracy becomes possible further again. That is, it is because an approximation property can be brought close to a true value by increasing selection and calibration mark of the location of a proofreading point.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] In case the conventional monitor calibration circuit performs the monitor of two or more nonlinear electrical potential differences and a current value, it has the problem which needs the number of reverse property amendment circuits which carries out a monitor. That is, it is because the property of a detection electrical potential difference is different with a difference of each monitor value, for example, a sensing element, and the difference in the detection approach.
[0004] Moreover, in case two or more monitors are performed, in order to choose a monitor item as it is also with hand control by a switch etc., there is a problem which cannot display simultaneously two or more monitor points (signal to carry out). That is, a number of the class of signal of meter which carry out a monitor for indicating by simultaneous is required of analog meter, and even when having amended in digital value, it is for choosing the amendment circuit of two or more reverse properties.
[0005] The object of this invention is offering the monitor calibration circuit which proofreads two or more monitor point as it is also in one circuit at digital value, and is displayed on the occasion of the monitor of two or more nonlinear electrical potential differences and a current value.

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MEANS

[Means for Solving the Problem] An A/D-conversion means by which the monitor calibration circuit by this invention changes two or more analog monitor input signals into a digital monitor signal in time sharing, A memory means to store said digital monitor signal temporarily, and a calibration data storage means to store the calibration data which proofread said digital monitor signal, A calibration processing means to proofread said digital monitor signal by which reading appearance was carried out from said temporary storage means based on said corresponding calibration data, It is characterized by including the display means which inputs the digital monitor signal with which the plurality corresponding to said two or more analog monitor input signals was proofread in time sharing, and indicates by package.
[0007] Moreover, it is characterized by said calibration processing means proofreading said digital monitor signal by linear approximation, is further characterized by said calibration data storage means being constituted by the programmable ROM component eliminable electric, and is characterized by storing said calibration data in said calibration data storage means through said A/D-conversion circuit further again.
[0008] The operation of this invention is as follows. By control from a microprocessor circuit, two or more analog input signals are changed into digital value in time sharing, and are saved in a memory circuit. Moreover, it has the calibration data store circuit and drop for proofreading, and calibration processing and display processing to a drop are performed simultaneous in the microprocessor circuit which performs time-sharing processing.
[0009] It is not necessary to prepare the reverse property calibration circuit for every input signal by processing an analog input signal to time sharing in a microprocessor circuit. Since the circuit which performs calibration processing is one circuit, high-speed processing is possible. By performing time series processing at high speed, it is possible to always update two or more monitor values, and the package display of drops, such as a liquid crystal display, is attained in two or more monitor values.
[0010]
[Embodiment of the Invention] Below, the example of this invention is explained with reference to a drawing.
[0011] Drawing 1 is the block diagram showing the configuration of the example of the monitor calibration circuit by this invention. In drawing 1 , the monitor calibration circuit by this invention has A/D converter 1 which carries out the analog / digital (A/D) conversion of the analog monitor input signals CH1-CH8 of eight channels in time sharing, the microprocessor circuit (central processing unit;CPU; computer) 2 which controls the whole monitor calibration circuit, and RAM (random access memory)3 which stores temporarily the digital monitor signal b of the output of an A/D converter.
[0012] Moreover, the calibration processing calibration processing circuit 5 based on EEPROM (a programmable ROM eliminable electric; calibration data store circuit)4 which stores calibration data, and the calibration data d by which reading appearance was carried out from the calibration data store circuit 4 in the digital monitor signal c, and the proofread digital monitor signal e are displayed, for example, it has the drops 6, such as a liquid crystal display in which a multi-line display is possible, and is constituted.

[0013] Drawing 1 explains actuation of the example of this invention. In drawing 1 , eight kinds of analog input electrical potential differences CH1-CH8 are inputted into A/D converter 1. CPU2 inputs the channel-control signal a into A/D converter 1, transforms the analog input electrical potential differences CH1-CH8 of an assignment channel to the digital value of a hexadecimal (hexa decimal), and is made to output as a digital monitor signal b by A/D converter 1.
[0014] The outputted digital monitor signal b is memorized by RAM3 through a data bus. By specifying the address with which the digital monitor signal b is memorized, CPU2 is managed so that the storage location with the digital monitor signal b of other channels may not overlap. CPU2 performs this processing by time-sharing high-speed processing, and memorizes it as hexa decimal data to RAM3 about all the analog input electrical potential differences CH1-CH8.
[0015] After storage of the digital monitor signal b to RAM3 of all channels is completed, calibration processing of the digital monitor signal c by the proofreading processing circuit 5 is started from the channel memorized first, and renewal of sequential of the stored data of RAM3 is carried out. By the calibration processing circuit 5, CPU2 performs linearity amendment processing simultaneously by parallel processing or time-sharing processing. CPU2 inputs the digital monitor signal c of an assignment channel into the calibration processing circuit 5 which consists of ejection and ROM (read-only memory) from RAM3.
[0016] The calibration processing circuit 5 uses the calibration data d memorized by the calibration data EEPROM 4, and performs calibration processing by making this into a criteria monitor value. The calibration data to each monitor signals CH1-CH8 are memorized by EEPROM4. The calibration data d divided the value to the full scale of each monitor point at the section of arbitration, established the proofreading point, and has set up calibration hexa decimal data for every proofreading point of the.
[0017] An example of calibration data is shown in drawing 3 . In drawing 3 , n is a proofreading point number (1 n= 0, 2 ..... n), An is decimal numeral data of the proofreading point n, and Bn is hexadecimal calibration data corresponding to the decimal number data of the proofreading point n. However, it is shown that the figure to which h is added is a figure of a hexadecimal (hexa decimal). It returns to drawing 1 , the digital monitor signals c (hexa decimal data) and Bn inputted first are compared in the calibration processing circuit 5 which consists of ROM, and it computes between which proofreading points the data is located. When the location P is n<P<n +1, the calibration output value (M) e outputted from the calibration processing circuit 5 becomes M=An+{(<C>d-<Bn>d) /(<Bn+1> d-<Bn>d)} x (An+1-An). however, the digital monitor signal (hexa decimal data) c with which C is memorized by RAM3 -- it is -- < -- >d is conversion to a decimal number from a hexadecimal.
[0018] Consequently, in the computed proofreading point section, linear approximation of the calibration output value (M) e is carried out. The example of linear approximation is shown in drawing 2 . In drawing 2 , a calibration output (display) value (electrical potential difference) (Vn) corresponds to the proofreading point data An (Bn) (refer to drawing 3), and linear approximation of the point P on the continuous line corresponding to the digital monitor input signal C (data) is carried out the point M on a broken line. A proofreading point and calibration mark are determined according to the meter error as which the difference (Vm-****) of this P and M is a meter error, and is required.
[0019] Returning to drawing 1 , the input of the digital monitor signal (hexa decimal data) c for every channel to the calibration processing circuit 5 which consists of a ROM is inputted by CPU2 from RAM3 in time sharing, and outputs the calibration output value (M) e for every channel from the calibration processing circuit 5. The calibration output value (M) e outputted from the calibration processing circuit 5 is sent to the LCD display 6 by time-sharing processing by CPU2, and indicates each monitor value by package.
[0020] The input of Bn (hexadecimal calibration data corresponding to the decimal numeral data of the proofreading point n) to EEPROM4 is also performed from an A/D converter, and is memorized by direct EEPROM4 by CPU. This actuation is carried out for every channel.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram of the example of this invention.
[Drawing 2] It is the explanatory view of an example of the example of linear approximation.
[Drawing 3] It is the explanatory view of an example of calibration data.
[Description of Notations]
1 A/D Converter
2 CPU
3 RAM
4 Calibration Data Store Circuit
5 Calibration Processing Circuit
6 Drop

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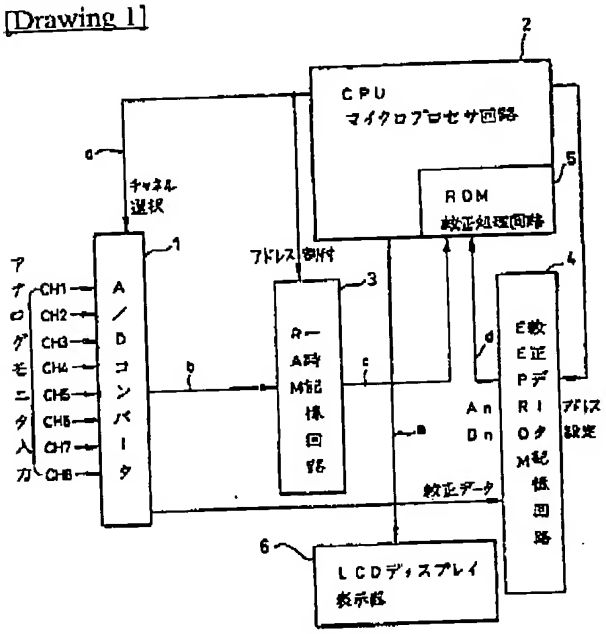
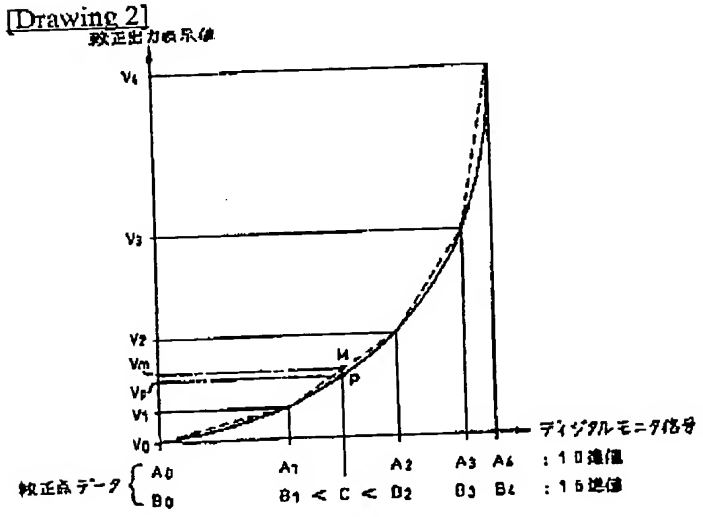
DRAWINGS

[Drawing 1]



[Drawing 2]



[Drawing 3]

n	0	1	2	. . . . .	n−1	n
An	0	5	10	. . . . .	95	100
Bn	000h	005h	010h	. . . . .	3D0h	3FFh
Vn	Vo	V1	V2	. . . . .	Vn-1	Vn

[Translation done.]